MEMORY CELL FOR MODIFICATION OF DEFAULT REGISTER VALUES IN AN INTEGRATED CIRCUIT CHIP

ABSTRACT OF THE DISCLOSURE

[00111] A memory cell circuit for modification of a default register value in an integrated circuit chip, which includes a plurality of metal layers and first and second supply potentials. The circuit comprises a memory cell, a register and a control circuit. The memory cell has a first metal interconnect structure that traverses the plurality of metal layers using a first plurality of vias, wherein the first metal interconnect structure is coupled to one of the first and second supply potentials, a second metal interconnect structure that traverses the plurality of metal layers using a second plurality of vias, wherein the second metal interconnect structure is coupled to the other one of the first and second supply potentials, and an output, wherein a state of the output is programmable by altering any one of the plurality of metal layers or any one of a plurality of via layers. The register has a data input, a data output and control inputs. The control circuit is coupled to the control inputs of the register. The control circuit receives a chip reset signal and the memory cell output to thereby force the data output of the register to a default register value that equals the output of the memory cell, regardless of the data input of the register.